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EXAMINER	
WANG, ALBERT C	
ART UNIT	**PAPER NUMBER**
2115	

DATE MAILED: 08/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/894,909	DALRYMPLE ET AL.	
	Examiner	Art Unit	
	Albert Wang	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-55 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-55 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 25 September 2001 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 9/25/01.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Original claims 1-55 are pending.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 2, 50, and 51 are rejected under 35 U.S.C. 102(b) as being anticipated by Kawaguchi, U.S. Patent No. 5,822,572.

As per claim 1, Kawaguchi discloses an apparatus for executing application programming at reduced circuit power consumption levels, comprising:

(a) a processing element (Fig. 1, CPU 104); and

(b) means for modulating the clock speed of said processing element under the control of an application program executable on said processing element (Col. 3, lines 33-47, CPU 104 is programmed to switch operating frequency; Col. 1, lines 36-46, operating frequency is the clock speed of the CPU).

As per claim 2, Kawaguchi discloses clock speed modulation means under program control is configured to allow the selection of at least two clock speeds (Col. 3, lines 8-23, selection of CLK1 or CLK2).

As per claim 50, Kawaguchi discloses a method of reducing power consumption within a processing element receiving an oscillator signal for driving its clock speed (Fig. 1, CPU 104 receives ORGCLK), comprising:

generating a processor clock speed control signal in response to programmed instructions being executed on said processing element (Col. 3, lines 33-47, CPU 104 is programmed to switch operating frequency; Col. 1, lines 36-46, operating frequency is the clock speed of the CPU); and

modifying the frequency of the oscillator signal in response to said processor clock speed signal (Col. 1, lines 47-53, CPU divides original clock to obtain operating frequency; Claim 1).

As per claim 51, Kawaguchi discloses the modification of the frequency of the oscillator signal comprises dividing the incoming oscillator frequency (Col. 1, lines 47-53, CPU divides original clock to obtain operating frequency).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 3-6, 10-19, and 53 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kawaguchi as applied to claim 1 above, and further in view of Gulick et al., U.S. Patent No. 5,408,639 ("Gulick").

As per claim 3, Kawaguchi teaches dividing an incoming oscillator signal, which is received by said processing element (Fig. 1, CPU 104 receives ORGCLK; Col. 1, lines 47-53,

CPU divides original clock to obtain operating frequency; Claim 1), but does not expressly teach using a divider circuit. Gulick teaches a divider circuit configured to divide an incoming oscillator signal from which processor clock speed is derived (Fig. 3, CPU 36 receives from divider 34 the divided output of clock source 22). At the time of the invention, it would have been obvious to one of ordinary skill in the art to apply Gulick's divider circuit to Kawaguchi's dividing process. A motivation for doing so would have been to ensure the integrity of Kawaguchi's apparatus.

As per claim 4, Kawaguchi teaches dividing the incoming oscillator signal by a value greater than unity, such that the oscillator signal provided to the processor is less than the incoming oscillator frequency (Col. 1, lines 47-53; Col. 3, lines 8-23).

As per claim 5, Gulick teaches the divider circuit is configured to have at least one discrete division value that may be programmable (Col. 9, lines 39-50).

As per claim 6, Kawaguchi teaches the incoming oscillator signal may be divided by eight under program direction and supplied to the processing element (Col. 3, lines 8-23).

As per claims 10-13 and 53, Kawaguchi teaches the clock speed modulation means comprises a circuit configured to select an alternative oscillator signal for the processing element (Col. 6, lines 20-24).

As per claim 14, Gulick teaches integrating circuit means within a processing element (Fig. 4).

As per claim 15, Gulick teaches a plurality of chip selects (Fig. 3) and Kawaguchi teaches:

(a) means for modifying the duration of peripheral device chip selects being output by said processing element (Figs. 1 & 3, timing circuit 102 outputs /NewCS and /NewOE to peripheral circuit 106); and

(b) said chip select duration modifying means configured to change duration of at least one chip select signal in response to the selected clock speed of the processor such that peripheral access timing requirements are met while limiting the power consumption of the peripheral device associated with device selection (Figs. 5 & 6, ratio of /NewCS to CLK2 is smaller than that of /CS to CLK1)

As per claims 16 and 17, Kawaguchi teaches the chip select duration modification means comprises a digital circuit which receives processor timing signals and at least one conventional chip select signal from which it generates a power-saving chip select signal having a relative duration which is responsive to changes in processor clock speed (Figs. 3 & 4, timing circuit 102 receives SYSCLK and /CS; Claims 1, 4 and 7, active time percentage of chip select signal is altered according to operating frequency)

As per claim 18, Kawaguchi teaches the digital circuit for modifying chip select duration comprises latching circuitry for sufficiently retaining data integrity according to the timing of the power-saving chip select signal (Fig. 4).

As per claim 19, Gulick teaches integrating circuits within a processing element (Fig. 4).

4. Claims 20-23, 25-42, 44-49, 54 and 55 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kawaguchi, U.S. Patent No. 5,822,572, in view of Gulick et al., U.S. Patent No. 5,408,639 ("Gulick").

As per claim 20, Kawaguchi teaches in a processing element configured for operation at a clock speed as derived from an oscillator (Fig. 1, CPU 104 receives ORGCLK), wherein the improvement comprises:

(a) an oscillator frequency modification means (Col. 1, lines 47-53, CPU divides original clock to obtain operating frequency; Claim 1);

(b) said oscillator frequency modification means being configured to modify the frequency received by the processing element as an execution clock (Col. 1, lines 36-46, operating frequency is the clock speed of the CPU); and

(c) said oscillator frequency modification circuit is configured to respond to the programmed instructions executing on said processing element to allow changing processor execution speed (Col. 3, lines 33-47, CPU 104 is programmed to switch operating frequency).

However, Kawaguchi does not expressly teach said oscillator frequency modification means as a circuit. Gulick teaches a divider circuit configured to divide an incoming oscillator signal from which processor clock speed is derived (Fig. 3, CPU 36 receives from divider 34 the divided output of clock source 22). At the time of the invention, it would have been obvious to one of ordinary skill in the art to apply Gulick's divider circuit as Kawaguchi's oscillator frequency modification means. A motivation for doing so would have been to ensure the integrity of Kawaguchi's processing element.

As per claim 21, Kawaguchi teaches the processing element is an electronic circuit or device capable of executing programmed instructions as selected from the group of devices and circuits consisting of microprocessors, microcontrollers, digital-signal processors, and central processing units (Col. 6, lines 24-30).

As per claim 22, Gulick teaches the oscillator frequency modification circuit comprises a selective oscillator divider circuit, which divides an incoming oscillator signal under program control to be utilized as the clock within the processing element (Fig. 3; Col. 9, lines 39-50).

As per claim 23, Kawaguchi teaches dividing the incoming oscillator signal by a value greater than unity when directed by the executing program, such that the clock speed of the processing element may be reduced (Col. 3, lines 8-23).

As per claim 25, Kawaguchi teaches the oscillator frequency modification circuit comprises an oscillator selection circuit configured to allow the selection of at least one alternative oscillator under program control to be utilized as the clock within the processing element (Col. 6, lines 20-24).

As per claim 26, Kawaguchi teaches the oscillator frequency modification circuit is integrated within the processing element (Fig. 1; Col. 3, lines 8-23).

As per claim 27, Kawaguchi teaches in an electronic circuit containing a processor element configured for operation at more than one clock frequency, and to which chip select outputs are interfaced to a peripheral device, wherein the improvement comprises:

(a) a chip select timing circuit which generates a signal in response to processor element clock frequency and timing (Figs. 1 & 3, decoder 103 generates signal; Col. 3, lines 8-23 & 33-47, in response to operating frequency); and

(b) a gating circuit which receives a signal from said chip select timing circuit and in response alters the percentage interval over which chip select outputs to the peripheral device

are active (Figs. 1 & 3, timing circuit 102 outputs /NewCS and /NewOE to peripheral circuit 106; Claims 1, 4 and 7, active time percentage of chip select signal is altered according to operating frequency).

However, Kawaguchi does not expressly teach outputting chip select outputs to a plurality of peripheral devices. Gulick teaches outputting chip select signals to memory devices (Fig. 3, output 68 over lines 70 to memories 28 and 30; Col. 8, lines 25-47, output 68 conveys chip select signals). At the time of the invention, it would have been obvious to one skilled in the art to substitute Gulick's plurality of memories for Kawaguchi's peripheral circuit. A motivation for doing so would have been to ensure the integrity of Kawaguchi's electronic circuit when applied to other types of peripheral circuits (Kawaguchi Col. 6, lines 4-19; Gulick Col. 2, lines 33-49).

As per claim 28, Kawaguchi teaches the processing element is an electronic circuit or device capable of executing programmed instructions as selected from the group of devices and circuits consisting of microprocessors, microcontrollers, digital-signal processors, and central processing units (Co. 6, lines 24-30).

As per claims 29, Gulick teaches the peripheral devices comprise memory devices (Fig. 3).

As per claim 30, Gulick teaches the memory devices comprise static memory integrated circuits (Col. 2, lines 33-49).

As per claim 31, Gulick teaches integrating circuits within a processing element (Fig. 4).

As per claim 32, Kawaguchi teaches a circuit for modulating the duration of a chip select signal in association with a processor element capable of operating with a selectable cycle clock, comprising:

(a) a processor clock speed detection circuit (Col. 3, lines 33-47, comprising "predetermined internal register");

(b) a chip selection restriction circuit connected to said clock speed detection circuit (Figs. 1 & 3, decoder 103);

(c) said chip selection restriction circuit receiving one or more signals associated with said processor element and configured to generate a restricted chip select signal in response to processor clock speed (Figs. 1 & 3, decoder 103 receives via AD BUS and generates mode I/O signal; Col. 3, lines 24-47); and

(d) a chip select gating circuit which receives said restricted chip select signal for modulating at least one chip select output signal to at least one peripheral device of the processing element (Figs. 1 & 3, timing circuit 102 outputs chip select signal to peripheral circuit 106; Figs. 5 & 6, ratio of /NewCS to CLK2 is smaller than that of /CS to CLK1).

However, Kawaguchi does not expressly teach outputting a plurality of chip select signals. Gulick teaches outputting chip select signals to memory devices (Fig. 3, output 68 over lines 70 to memories 28 and 30; Col. 8, lines 25-47, output 68 conveys chip select signals). At the time of the invention, it would have been obvious to one skilled in the art to substitute Gulick's plurality of memories for Kawaguchi's peripheral circuit. A motivation for doing so would have been to ensure the integrity of Kawaguchi's electronic circuit when applied to other types of peripheral circuits (Kawaguchi Col. 6, lines 4-19; Gulick Col. 2, lines 33-49).

As per claim 33, Kawaguchi teaches said chip selection restriction circuit is configured to generate an output responsive to selected periods of the oscillator clock within a given instruction cycle (Figs. 5 & 6).

As per claim 34, Kawaguchi teaches the selected periods of said oscillator clock comprise a given multiple of periods at a predetermined position within a given instruction cycle (Figs. 5 & 6).

As per claim 35, Kawaguchi teaches selected periods comprise the last two periods within a given instruction cycle (Figs. 5 & 6, 8 & 9, 11 & 12, periods may be altered).

As per claim 36, Kawaguchi teaches said chip selection restriction circuit is configured with a timer circuit that generates a signal of predetermined duration as triggered by a processor signal (Figs. 5 & 6).

As per claim 37, Kawaguchi teaches the timer circuit is triggered by an output enable signal from the processor element (Fig. 3).

As per claim 38, Kawaguchi teaches the chip select gating circuit logically combines said restricted chip select signal to conventional peripheral chip select signals to generate new power-saving peripheral chip selects whose relative duration is responsive to processor clock speed (Claims 1, 4 and 7, active time percentage of chip select signal is altered according to operating frequency; Figs. 5 & 6, ratio of /NewCS to CLK2 is smaller than that of /CS to CLK1).

As per claim 39, Kawaguchi teaches the logical combination comprises ANDing of a conventional chip select signal with that of the restricted chip select signal to generate the new power-saving peripheral chip select (Fig. 4).

As per claim 40, Kawaguchi teaches a circuit for reducing the operating current for devices which interface to a processing element that utilizes a selectable frequency processor clock, comprising:

(a) a chip select timing circuit which interfaces with said processing element (Figs. 1 & 3, coder 103 interfaces CPU 104);

(b) said chip select timing circuit receiving at least one signal indicative of the selected frequency of the processor clock (Figs. 1 & 3, decoder 103 receives via AD BUS; Col. 3, lines 24-47);

(c) said chip select timing circuit receiving at least one timing conditioning signal (Fig. 3, data signal);

(d) said chip select timing circuit logically combining said received signals into a chip select restriction signal (Fig. 3);

(e) a gating circuit which utilizes the chip select restriction signal to gate at least one received chip select signal (Fig. 3, timing circuit 102 gates /CS); and

(f) said gating circuit generating an altered chip select signal that have a timing and pulse width configured in response to processor element clock speed (Claims 1, 4 and 7, active time percentage of chip select signal is altered according to operating frequency; Figs. 5 & 6, ratio of /NewCS to CLK2 is smaller than that of /CS to CLK1).

However, Kawaguchi does not expressly teach generating a plurality of chip select signals. Gulick teaches outputting chip select signals to memory devices (Fig. 3, output 68 over lines 70 to memories 28 and 30; Col. 8, lines 25-47, output 68 conveys chip select signals). At the time of the invention, it would have been obvious to one skilled in the art to substitute

Gulick's plurality of memories for Kawaguchi's peripheral circuit. A motivation for doing so would have been to ensure the integrity of Kawaguchi's electronic circuit when applied to other types of peripheral circuits (Kawaguchi Col. 6, lines 4-19; Gulick Col. 2, lines 33-49).

As per claim 41, Gulick teaches the signal indicative of the selected frequency of the processor clock comprises a division value (Fig. 3).

As per claim 42, Kawaguchi teaches the processing element is configured for a selectable frequency processor clock by dividing a received clock signal for use as a cycle clock (Col. 1, lines 47-53; Col. 3, lines 8-23).

As per claims 44 and 45, Kawaguchi teaches the processing element is configured for a selectable frequency processor clock to allow the selection of an alternate oscillator input to drive the processor clock (Col. 6, lines 20-24).

As per claim 46, Kawaguchi teaches in an electronic circuit containing a processor element configured for operation at more than one clock frequency, and to which chip select outputs are interfaced to a peripheral device, wherein the improvement comprises:

a chip select timing circuit which generates a signal in response to processor element clock frequency and timing (Figs. 1 & 3, decoder 103 generates mode I/O signal; Col. 3, lines 24-47); and

a gating circuit which receives a signal from said chip select timing circuit and in response alters the percentage interval over which chip select outputs to the peripheral device are active (Figs. 1 & 3, timing circuit 102 outputs chip select signal to peripheral circuit 106; Figs. 5 & 6, ratio of /NewCS to CLK2 is smaller than that of /CS to CLK1).

However, Kawaguchi does not expressly teach outputting chip select outputs to a plurality of peripheral devices. Gulick teaches outputting chip select signals to memory devices (Fig. 3, output 68 over lines 70 to memories 28 and 30; Col. 8, lines 25-47, output 68 conveys chip select signals). At the time of the invention, it would have been obvious to one skilled in the art to substitute Gulick's plurality of memories for Kawaguchi's peripheral circuit. A motivation for doing so would have been to ensure the integrity of Kawaguchi's electronic circuit when applied to other types of peripheral circuits (Kawaguchi Col. 6, lines 4-19; Gulick Col. 2, lines 33-49).

As per claim 47, Kawaguchi teaches the processing element is an electronic circuit or device capable of executing programmed instructions as selected from the group of devices and circuits consisting of microprocessors, microcontrollers, digital-signal processors, and central processing units (Co. 6, lines 24-30).

As per claim 48, Gulick teaches the peripheral devices comprise memory devices (Fig. 3).

As per claim 49, Gulick teaches the memory devices comprise static memory integrated circuits (Col. 2, lines 33-49).

As per claim 54, Kawaguchi teaches a method of reducing power consumption in a circuit containing a processing element configured for multiple clock speed operation which is interfaced to a peripheral device, comprising:

generating a processor speed selection signal that is responsive to the selection of processor element clock speed (Col. 3, lines 33-47, CPU 104 is programmed to switch operating frequency; Col. 1, lines 36-46, operating frequency is the clock speed of the CPU);

deriving a chip select restriction signal from the processor speed selection signal and timing signals within said processor element (Figs. 1 & 3, decoder 103 receives via AD BUS and generates mode I/O signal; Col. 3, lines 24-47); and

gating chip select signals communicated to the peripheral devices with the chip select restriction signal to modulate the active periods of the peripheral device to provide for reduced levels of power consumption (Figs. 1 & 3, timing circuit 102 outputs chip select signal to peripheral circuit 106; Figs. 5 & 6, ratio of /NewCS to CLK2 is smaller than that of /CS to CLK1).

However, Kawaguchi does not expressly teach outputting chip select outputs to a plurality of peripheral devices. Gulick teaches outputting chip select signals to memory devices (Fig. 3, output 68 over lines 70 to memories 28 and 30; Col. 8, lines 25-47, output 68 conveys chip select signals). At the time of the invention, it would have been obvious to one skilled in the art to substitute Gulick's plurality of memories for Kawaguchi's peripheral circuit. A motivation for doing so would have been to ensure the integrity of Kawaguchi's electronic circuit when applied to other types of peripheral circuits (Kawaguchi Col. 6, lines 4-19; Gulick Col. 2, lines 33-49).

As per claim 55, Kawaguchi teaches the duration of the chip select restriction signal is derived from a timer circuit triggered by timing signal within said processing element (Fig. 3).

5. Claims 7-9, 24, 43, and 52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kawaguchi/Gulick as applied to claims 3, 22, 40, and 50 above, and further in view of Rabbit Semiconductor, "Rabbit 2000 Microprocessor Designer's Handbook", 2000 ("Rabbit").

As per claims 7-9, 24, 43, and 52, Kawaguchi/Gulick does not expressly teach the oscillator signal provided to the processor is greater than the incoming oscillator frequency. Rabbit teaches multiplying the incoming oscillator frequency (Fig. 13). At the time of the invention, it would have been obvious to one of ordinary skill in the art to apply Rabbit's multiplying the incoming frequency to Kawaguchi/Gulick's system, in order to facilitate switching between power levels.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Albert Wang whose telephone number is 703-305-5385. The examiner can normally be reached on M-F (9:30 - 6:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on 703-305-9717. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

aw
August 18, 2004

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